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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/497,916	02/04/2000	Antonino Torres	S1022/8385	8061

7590 10/27/2003

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/497,916	TORRES ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19 and 20* is/are allowed.

6)☒ Claim(s) *1-11,13-16 and 18* is/are rejected.

7)☒ Claim(s) *12 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, an emitter of the first bipolar transistor being directly connected to the isolation region, as recited in claims 12 and 17, must be shown in figure 7 or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11, 13-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiello et al. (5,382,837).

Regarding claims 1 and 14, Aiello et al. teach in figures 6 and 10 an integrated circuit including a vertical power bipolar transistor having a terminal formed by a chip substrate of a first conductivity type 53, a control circuit thereof, the control

circuit isolated from the substrate by means of an isolation region 5, 34 of a second conductivity type, and a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor T2 with an emitter connected to the isolation region (via base and collector regions) and a collector connected to a reference potential input of the integrated circuit (via transistor T1), a bias circuit T4 for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor T3 with an emitter directly connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential and the first bipolar transistor is off.

Regarding the claimed limitations of coupling an isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential, Aiello et al. teach in figure 10 an isolation region 5, 34 coupled to substrate 53 through a high-impedance n- region 4. This connection remains when the substrate potential is lower than the reference potential. Therefore, Aiello et al. teach an isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential, as claimed.

Although Aiello et al. do not teach using the device as a protection structure against polarity inversion of a substrate potential wherein the bias circuit biases the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, this feature is inherent in Aiello et

al.'s device, because Aiello et al.'s structure is identical to the claimed structure. Note that the recitation of using the device as a protection structure against polarity inversion of a substrate potential has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Therefore, the claimed structure is considered to be at least obvious over Aiello et al.'s structure.

In the alternative, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Aiello et al.'s device as a protection structure against polarity inversion of a substrate potential wherein the bias circuit biases the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential in order to use the device in an application which requires a protection circuit.

Regarding claim 2, Aiello et al. teach a bias circuit comprises a third bipolar transistor T4 with an emitter coupled to control terminal of the integrated circuit and a collector coupled to a base of the first bipolar transistor. Regarding the claimed limitations of using the control terminal to receive an external control signal which is used by the control circuit to cause switching of the power

component and providing a voltage supply to the control circuit and to the bias circuit, note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 3, Aiello et al. teach in figure 10 a first bipolar transistor is a vertical transistor having an emitter formed by the substrate, a collector formed by a second doped region of the first conductivity type, and a base formed by a first doped region of the second conductivity type formed in the substrate and within the first doped region.

Regarding claim 4, Aiello et al. teach first and third bipolar transistors are isolated from the substrate by the isolation region.

Regarding claim 5, it would be obvious for an artisan to use first conductivity type is the N type, the second conductivity type is the P type, the first and second bipolar transistors are NPN transistors, and the third bipolar transistor is a PNP transistor in Aiello et al.'s device, because it is conventional to reverse the polarity of the transistor.

Regarding claims 7 and 9, Aiello et al. teach in figures 6 and 10 an integrated circuit comprising a vertical power bipolar transistor having a terminal formed by a chip substrate of a first conductivity type 53, a control circuit thereof, the control circuit isolated from the substrate by means of an isolation region 5, 34 of a second conductivity type, and a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor T2 with an emitter connected to the isolation region (via base and collector regions) and a collector connected to a reference potential input of the integrated circuit (via transistor T1), a bias circuit T4 for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor T3 with an emitter connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential and the first bipolar transistor is off.

Aiello et al. do not teach using the device as a protection structure against polarity inversion of a substrate potential wherein the bias circuit biases the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Aiello et al.'s device as a protection structure against polarity inversion of a substrate potential in order to use the device in an application which requires a protection circuit.

Note that the recitation of using the device as a protection structure against polarity inversion of a substrate potential occurs in the preamble and a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 8, Aiello et al. teach a second bipolar transistor forms a regulation loop that reduces parasitic transistor action from affecting the first bipolar transistor and the bias circuit.

Regarding claims 10 and 15, Aiello et al. teach a first bipolar transistor couples the isolation region to a reference potential input. This connection remains when the substrate potential is higher than the reference potential. Therefore, Aiello et al. teach a first bipolar transistor couples the isolation region to a reference

potential input when the substrate potential is lower than the reference potential, as claimed.

Regarding claims 11 and 16, the first bipolar transistor is off when the substrate potential is less than the reference potential, because the reference potential can be chosen such that the first bipolar transistor is off when the substrate potential is less than the reference potential.

Regarding claims 13 and 18, the collector of the first bipolar transistor is directly connected to the reference potential input 1.

Allowable Subject Matter

3. Claims 19 and 20 are allowable.

4. Claims 12 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for allowance

5. The following is an examiner's statement of reasons for allowance: Aiello et al. appear to be the closest prior art reference. Aiello et al. teach substantially the entire claimed structure as recited in claims 1 and 7, except an

emitter of the first bipolar transistor being directly connected to the isolation region. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant argues that Aiello et al. do not teach a second bipolar transistor with an emitter directly connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential and the first bipolar transistor is off.

Aiello et al. teach in figure 10 an isolation region 5, 34 coupled to substrate 53 through a high-impedance n- region 4. This connection remains when the substrate potential is lower than the reference potential. Therefore, Aiello et al. teach an isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential, as claimed.

Furthermore, applicant recites that the second bipolar transistor Q22 (applicant's response on 3/8/2002, page 4, "regarding claim 5") includes a base 30 isolated from the isolation region (specification, page 6, lines 30-31). Claims

1 and 7 recite the base is coupled to the isolation region in order to (for) couple the isolation region to the substrate through a high-impedance. It seems that applicant uses the term "couple" broadly to describe isolation.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
October 25, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800